

**General Description**

The WSF4022 is the highest performance trench Dual N-Ch MOSFET with extreme high cell density, which provide excellent  $R_{DS(on)}$  and gate charge for most of the synchronous buck converter applications.

The WSF4022 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

**Features**

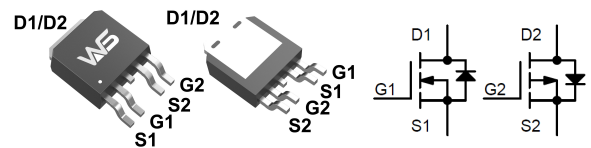
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent  $CdV/dt$  effect decline
- 100% EAS Guaranteed
- Green Device Available

**Product Summary**

$B_{V_{DS}}$	$R_{DSON}$	$I_D$
40V	21m $\Omega$	20A

**Applications**

- For Fan Pre-driver H-Bridge.
- Motor Control.
- Synchronous Rectification.

**TO-252-4L Pin Configuration**

**Absolute Maximum Ratings @ $T_A=25^\circ\text{C}$  unless otherwise noted**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current (Continuous) *AC	$T_C=25^\circ\text{C}$ 20*	A
$I_D$	Drain Current (Continuous) *AC	$T_C=100^\circ\text{C}$ 20*	A
$I_D$	Drain Current (Continuous) *AC	$T_A=25^\circ\text{C}$ 12.2	A
$I_D$	Drain Current (Continuous) *AC	$T_A=70^\circ\text{C}$ 10.2	A
$I_{DM}^a$	Pulsed Drain Current	$T_C=25^\circ\text{C}$ 80*	A
$E_{AS}^b$	Single Pulse Avalanche Energy	$L=0.5\text{mH}$ 25	mJ
$I_{AS}^b$	Avalanche Current	$L=0.5\text{mH}$ 17.8	A
$P_D$	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ 39.4	W
$P_D$	Maximum Power Dissipation	$T_C=100^\circ\text{C}$ 19.7	W
$P_D$	Power Dissipation	$T_A=25^\circ\text{C}$ 6.4	W
$P_D$	Power Dissipation	$T_A=70^\circ\text{C}$ 4.2	W
$T_J$	Operating Junction Temperature Range	175	$^\circ\text{C}$
$T_{STG}$	Operating Temperature/ Storage Temperature	-55~175	$^\circ\text{C}$
$R_{\theta JA}^b$	Thermal Resistance Junction-Ambient	Steady State <sup>c</sup> 60	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	3.8	$^\circ\text{C}/\text{W}$

Note \*: Limited by package.

Note a: Pulse width limited by max. junction temperature.

Note b: UIS tested and pulse width limited by maximum junction temperature  $175^\circ\text{C}$  (initial temperature  $T_j=25^\circ\text{C}$ ).

Note c: Surface Mounted on 1in2 pad area,  $t=999\text{sec}$ .

**Electrical Characteristics @ $T_A=25^{\circ}\text{C}$  unless otherwise noted**

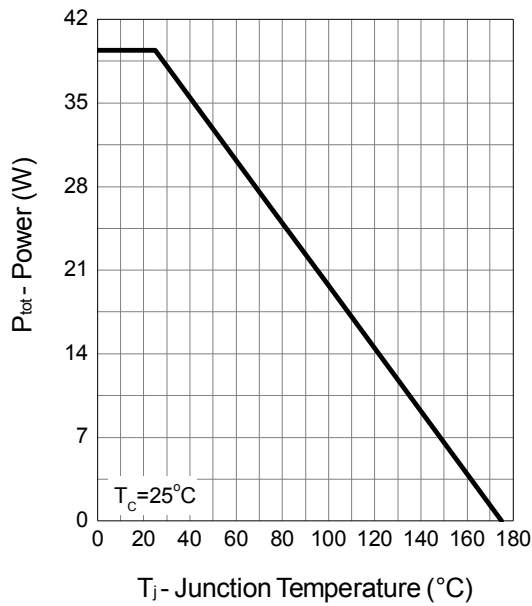
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	40			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V$			1	$\mu A$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V, T_J=85^{\circ}\text{C}$			30	$\mu A$
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{DS} = 250\mu A$	1.1	1.6	2.5	V
$R_{DS(on)}^d$	Drain-Source On-state Resistance	$V_{GS} = 10V, I_D = 10A$		16	21	m $\Omega$
		$V_{GS} = 4.5V, I_D = 5A$		18	25	m $\Omega$
Gate Charge <sup>e</sup>						
Qg	Total Gate Charge	$V_{DS}=20V, V_{GS}=4.5V, I_D=10A$		7.5		nC
Qgs	Gate-Source Charge			3.24		nC
Qgd	Gate-Drain Charge			2.75		nC
Dynamic <sup>e</sup>						
Ciss	Input Capacitance	$V_{GS}=0V, V_{DS}=20V, f=1\text{MHz}$		815		pF
Coss	Output Capacitance			95		pF
Crss	Reverse Transfer Capacitance			60		pF
td (on)	Turn-on Delay Time	$V_{DD}=20V, V_{GEN}=10V, I_{DS}=1A, R_G=6\Omega, R_L=20\Omega.$		7.8		ns
tr	Turn-on Rise Time			6.9		ns
td(off)	Turn-off Delay Time			22.4		ns
tf	Turn-off Fall Time			4.8		ns
Diode						
$V_{SD}^d$	Diode Forward Voltage	$I_{SD}=1A, V_{GS}=0V$		0.75	1.1	V
trr	Input Capacitance	$I_{DS}=10A, dl_{SD}/dt=100A/\mu s$		13		ns
Qrr	Output Capacitance			8.7		nC

Note d: Pulse test ; pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

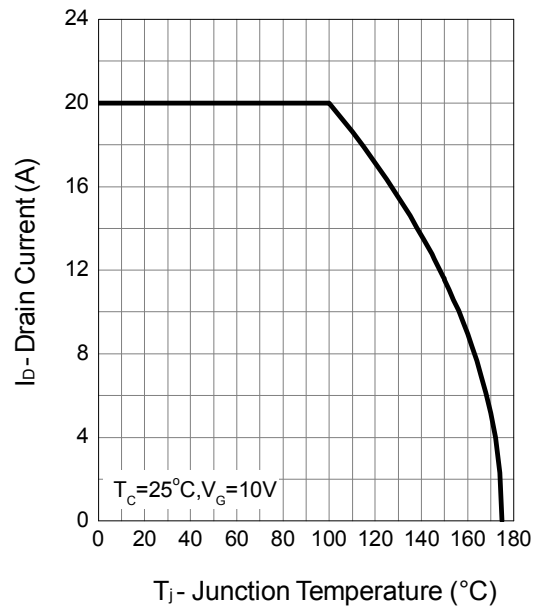
Note e: Guaranteed by design, not subject to production testing.

## Typical Characteristics

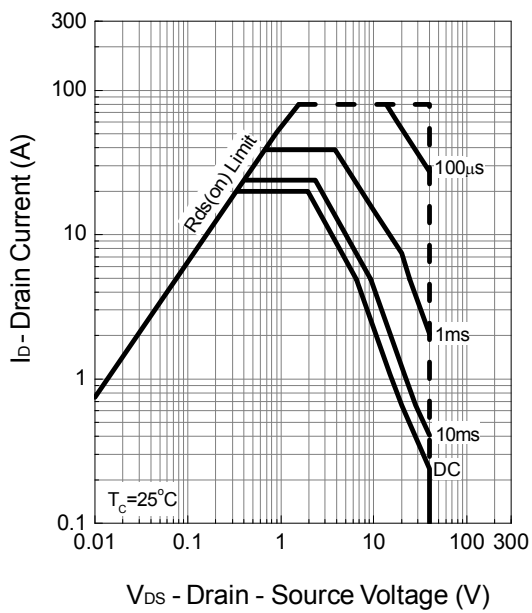
**Power Dissipation**



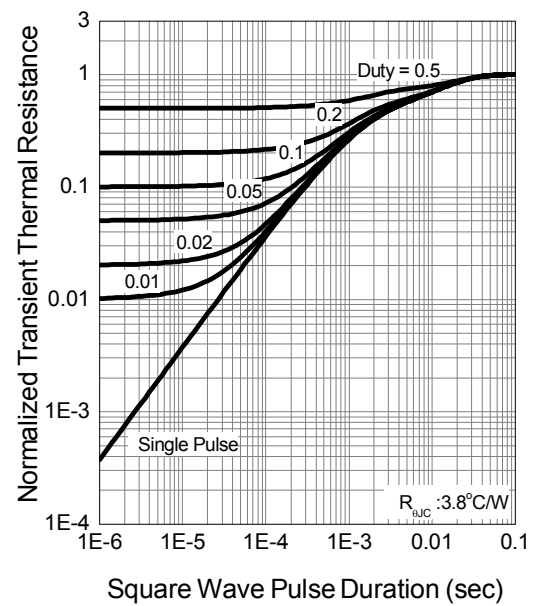
**Drain Current**



**Safe Operation Area**

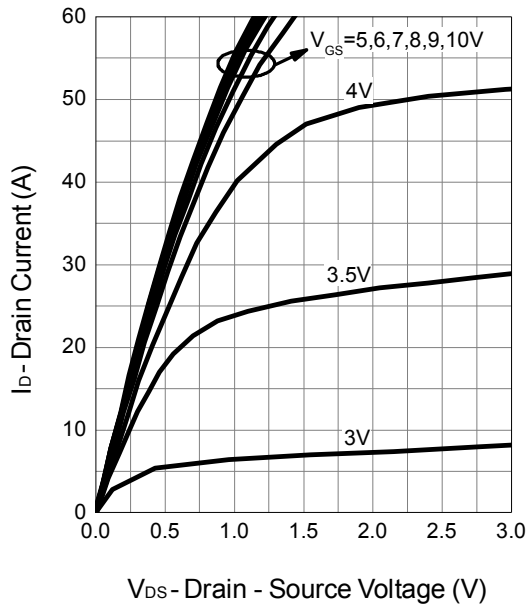


**Thermal Transient Impedance**

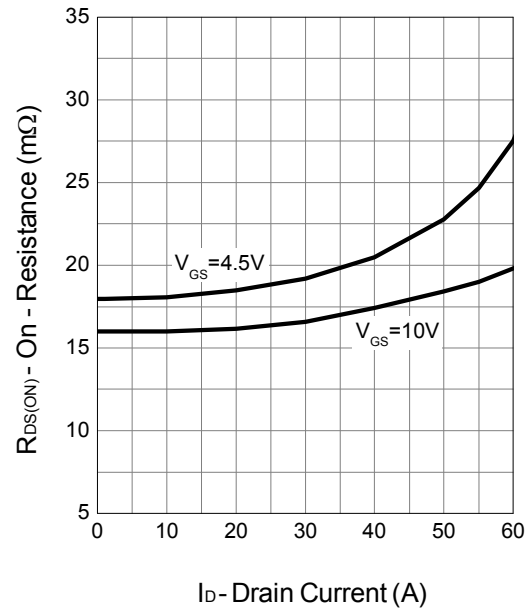


## Typical Characteristics

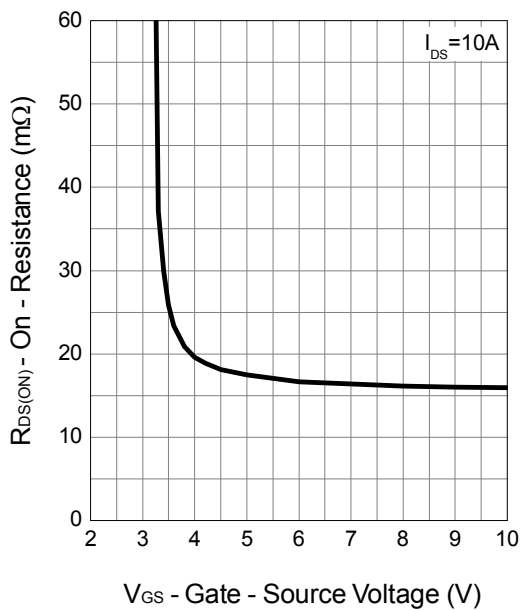
**Output Characteristics**



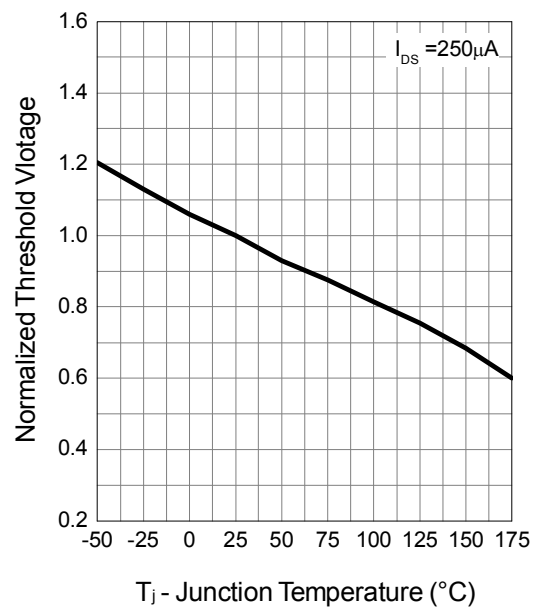
**Drain-Source On Resistance**



**Gate-Source On Resistance**

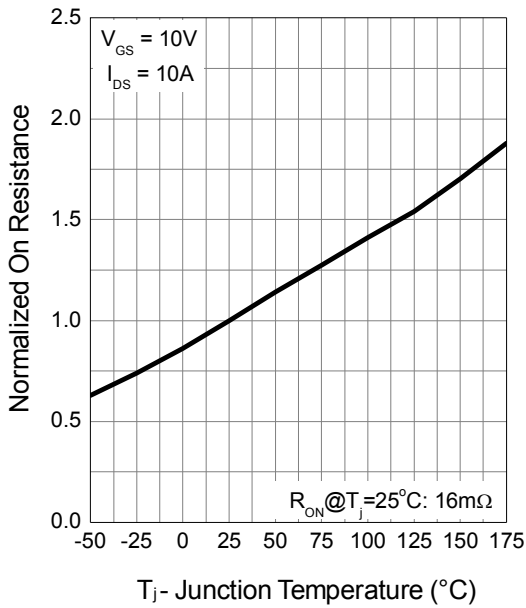


**Gate Threshold Voltage**

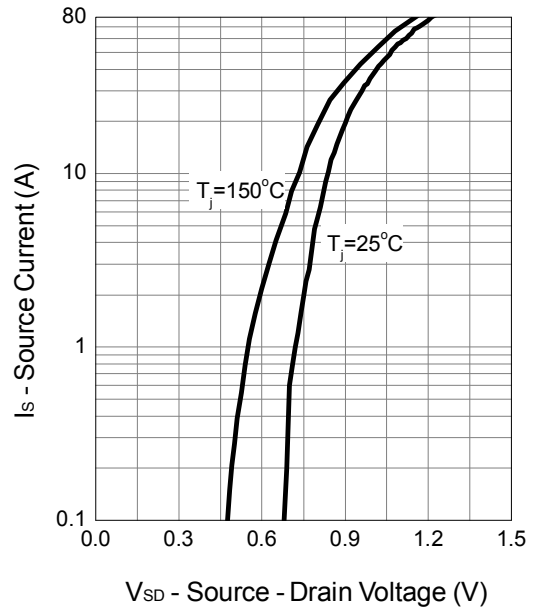


### Typical Characteristics

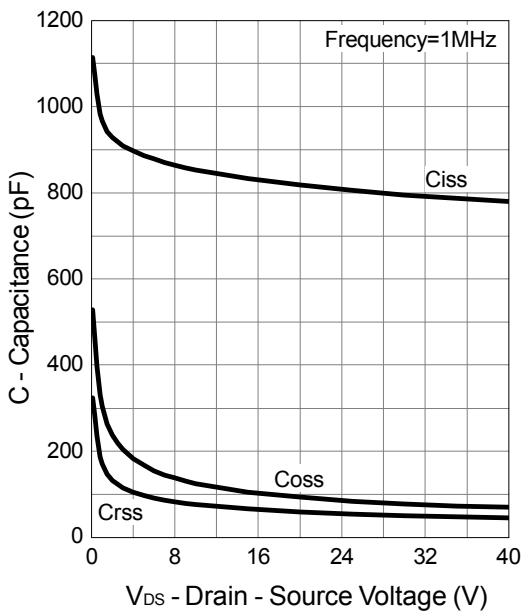
**Drain-Source On Resistance**



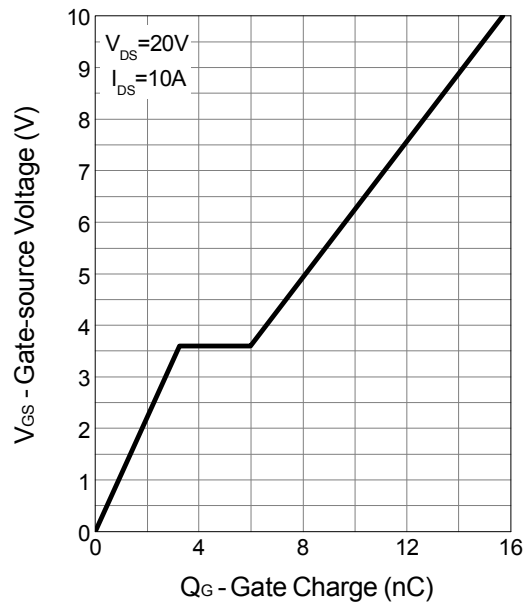
**Source-Drain Diode Forward**



**Capacitance**

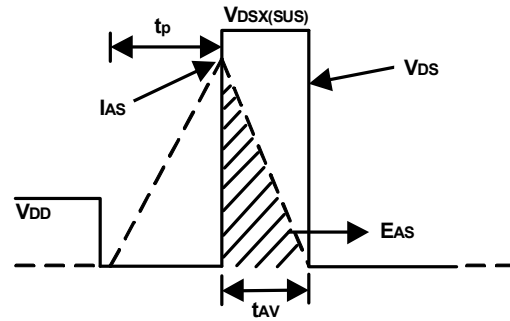
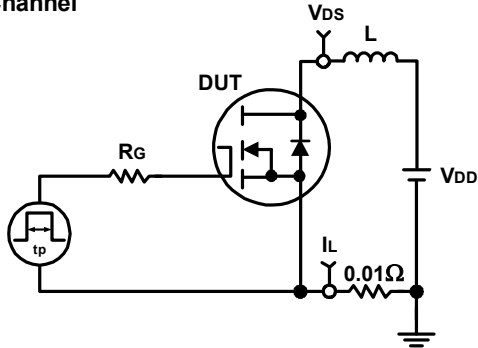


**Gate Charge**



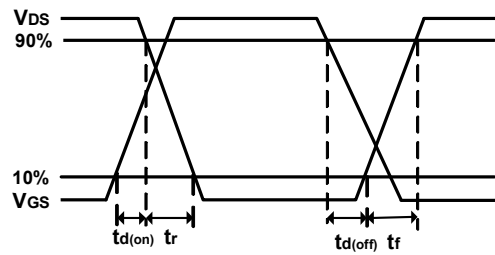
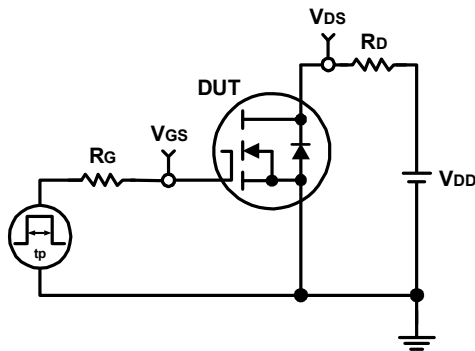
### Avalanche Test Circuit and Waveforms

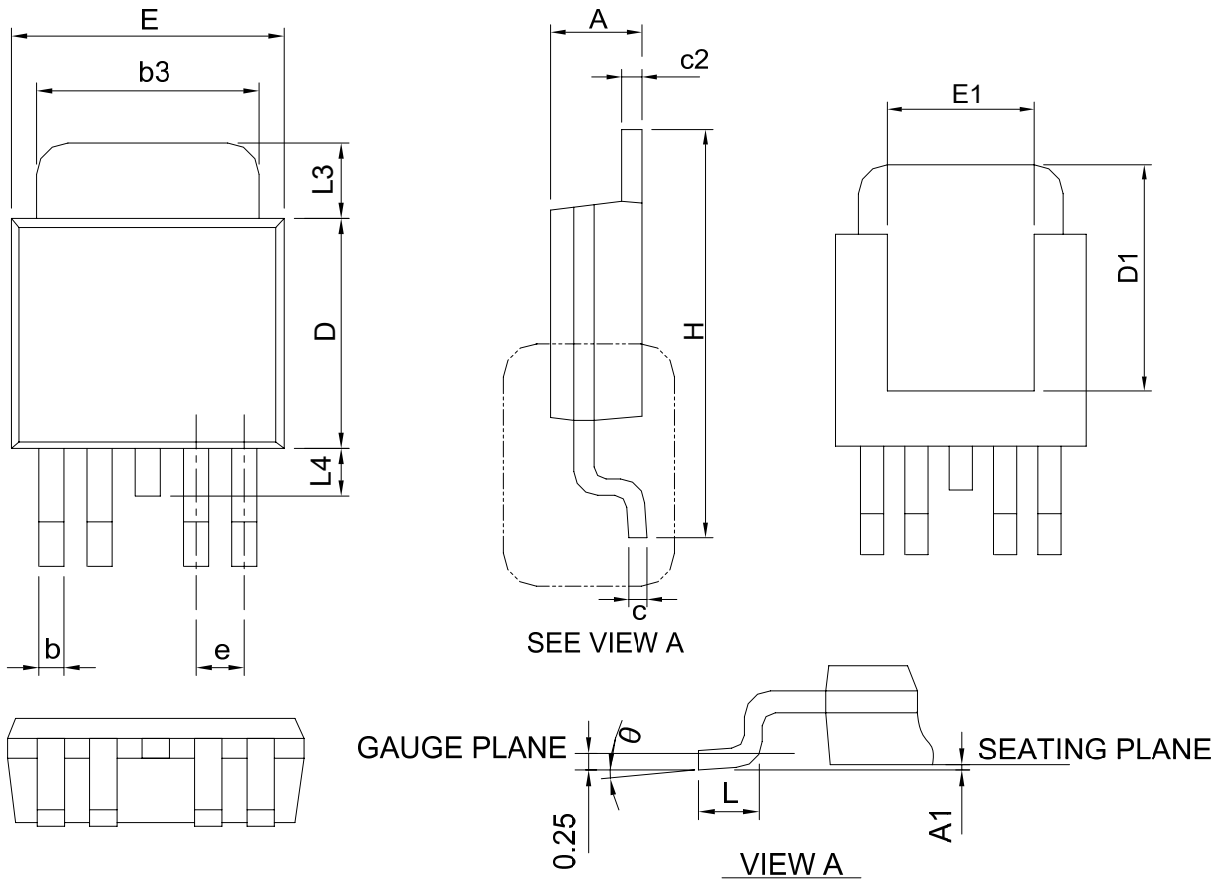
N Channel



### Switching Time Test Circuit and Waveforms

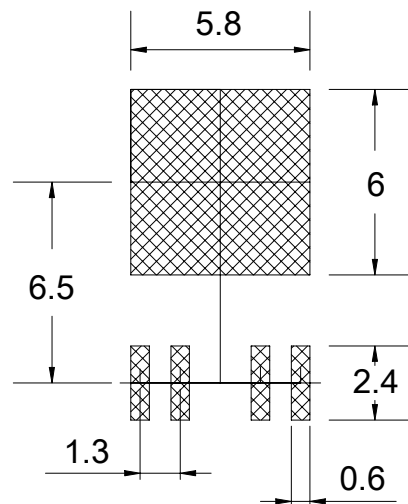
N Channel





SYMBOL	TO-252-4			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	-	0.2	-	0.008
b	0.50	0.71	0.020	0.028
b3	4.32	5.46	0.170	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	1.30 BSC		0.051 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L3	0.89	2.03	0.035	0.080
L4	-	1.02	-	0.040
θ	0°	8°	0°	8°

### RECOMMENDED LAND PATTERN



UNIT: mm



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